Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.129”**

**PAD FUNCTIONS:**

1. **V IN (2 bond pads)**
2. **V OUT (2 bond pads)**
3. **V OUT SENSE**
4. **ADJUST**

**.200”**

**ANODE**

**.200”**

**Top Material: TiNiAg**

**Backside Material: TiNiAg**

**Bond Pad Size: .191 X .191”**

**Backside Potential: CATHODE**

**APPROVED BY: DK DIE SIZE .200” X .200” DATE: 3/8/23**

**MFG: SILICON SUPPLIES THICKNESS .015” P/N: SIS200T200S**

**DG 10.1.2**

#### Rev B, 7/1